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10/689,716	10/22/2003	Nelson Gonzalez	19463-0002	3956

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,716	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7,29-34,41,42,44-48 and 50-52 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7,29-34,41,42,44-48 and 50-52 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In light of Applicant's amendment to Claim 44, the objection to this claim has been withdrawn.

2. Applicant's arguments with respect to claims 1-7, 29-34, 41, 42, 44-48, and 50-52 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see page 10, filed September 29, 2005, with respect to the rejection(s) of claim(s) 1-7, 29-34, 41, 42, 44-48, and 50-52 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Peleg (US006557065B1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7, 29-34, and 41, 42, and 44-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) in view of Peleg (US006557065B1).

7. With regard to Claim 1, Levy describes a chipset (104, Figure 1) for managing data transfers within the computing device [0014]; a scalable interconnect (Device 0) connecting to the computing device [0021]; and a plurality of ports or high-speed video card slots [0016] connected to the interconnect [0021], the high speed video card slots including at least one first video card slot and second video card slot [0016].

However, Levy does not teach that the computing device is a motherboard and that the motherboard enables a first and a second video card to attach, respectively, to the at least one first video card slot and second video card slot, and wherein the motherboard enables the first and the second video card to operate concurrently to output graphics data. However, Peleg describes a motherboard (16, Figure 3) that enables a first (60) and a second video card (200) to attach, respectively, to the at least one first video card slot (62) and second video card slot (205) (Col. 1, lines 40-57; Col. 4, lines 15-19). The second video card is a co-processor (Col. 4, lines 15-19), and a co-processor is a processor that operates concurrently with another processor.

Therefore, the motherboard enables the first and the second video card to operate concurrently to output graphics data.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Levy so that the computing device is a motherboard as suggested by Peleg. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new features to the machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. The motherboard, by enabling pluggable components, allows users to personalize a computer system depending on their applications and needs. The advantages of using a motherboard can be found in many publications, such as the howstuffworks website. It would have been obvious to modify the device so that the motherboard enables a first and a second video card to attach, respectively, to the at least one first video card slot and second video card slot, and wherein the motherboard enables the first and the second video card to operate concurrently to output graphics data as suggested by Peleg. Peleg suggests that since future system and processor designs will operate at speeds far above existing bus transmission speeds, the demand for ever faster bus systems will continue to grow. Therefore, it can be appreciated that a substantial need exists for a new, fast high bandwidth bus that is protocol independent and can couple multiple agents (Col. 2, lines 25-32).

8. With regard to Claim 2, Levy describes a switch (116, Figure 3) connected to the interconnect (Device 0), wherein the switch distributes bandwidth from the interconnect to the plurality of high-speed video card slots [0021, 0017, 0018, 0016].

9. With regard to Claim 3, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection, and wherein the switch (116, Figure 3) distributes bandwidth from the x16 connection to two x16 video card slots [0001, 0021, 0017, 0018, 0016].

10. With regard to Claim 4, Levy describes that the interconnect comprises at least a x32 connection [0001].

11. With regard to Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Figure 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

12. With regard to Claim 6, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001. 0016].

13. With regard to Claim 7, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a connection having at least 24 lanes, and wherein the interconnect is divided into a x8 connection between the chipset (104, Figure 1) and one of the plurality of high-speed video card slots and a x16 connection between the chipset and another of the plurality of high-speed video card slots [0001, 0016].

14. With regard to Claim 29, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses that the interconnect comprises a first x16 connection to the first video card slot and a second smaller-scaled connection to the second video card slot [0001, 0016].

15. With regard to Claim 30, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

16. With regard to Claim 31, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example of a first video card slot and a second video card slot both having the prespecified dimensions of a x4 link. Therefore, Levy discloses a first video card slot and a second video card slot having first prespecified dimensions [0001, 0016].

17. With regard to Claim 32, Levy describes ports or a peripheral slot connected to the interconnect (Device 0, Figure 2). In Figure 2, the peripheral slot is shown to have the prespecified dimensions a x8 link, and the first dimensions are for a x4 link and a x8 link [0020]. Therefore, Levy discloses a peripheral slot having second prespecified dimensions, wherein the second dimensions differs from the first dimensions.

18. With regard to Claim 33, Levy describes that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy discloses first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots.

19. With regard to Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

20. With regard to Claim 41, Levy describes a computing device for supporting multiple video cards, the computing device comprising a processor socket (104, Figure 1) adapted to receive a processor (102) [0014]; a scalable interconnect (Device 0) that provides data paths to the processor socket (Figure 1), wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017]; and video card slots connected to the interconnect, wherein each of the video card slots is specifically adapted for coupling to a video card [0021, 0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second video card to output graphics data. However, Peleg describes that the computing device is a motherboard (16, Figure 3; Col. 1, lines 40-43), the processor is a central processing unit (CPU) (10; Col. 1, lines 31-38), and the motherboard is capable of receiving and facilitating concurrent operation of a first (60) and a second video card (200) to output graphics data (Col. 1 lines 40-57; Col. 4, lines 15-19), as discussed in the rejection for Claim 1.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so that the processor is a CPU as suggested by Peleg. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. This can be found in many publications, such as the Webopedia Online Encyclopedia.

21. With regard to Claim 42, Levy gives the example of the video card slots all having the dimensions of a x4 link [0001]. Therefore, Levy discloses video card slots having substantially similar dimensions.

22. With regard to Claim 44, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses that each of the video card slots is configured to couple with a graphics card designed to be used with a x16 connection [0001, 0016].

23. With regard to Claim 45, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect (Device 0, Figure 1) comprising a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

24. With regard to Claim 46, Claim 46 is similar in scope to Claim 30, and therefore is rejected under the same rationale.

25. With regard to Claim 47, Claim 47 is similar in scope to Claim 32, and therefore is rejected under the same rationale.

26. With regard to Claim 48, Levy describes a high performance computer including a processor socket (104, Figure 1) adapted to receive the processor (102) [0014], a scalable interconnect (Device 0) that provides data paths to the processor (Figure 1), wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017], and a first and a second video slots, wherein the first and the second video slots connect to one or more of the data paths [0020], the first and the second video slots have a substantially similar physical configuration [0001], as discussed in the rejection for Claim 42, wherein the video slot physical configuration is selected to allow the first and the second video slots to accept a graphics card; and a first graphics card coupled to the first video slot [0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and a second graphics card coupled to the second video slot, wherein first and second video cards operate concurrently to output graphics data to a display device. However, Peleg describes that the computing device is a motherboard (16, Figure 3; Col. 1, lines 40-43), the processor is a central processing unit (CPU) (10; Col. 1, lines 31-38), and a second graphics card (200) coupled to the second video slot (205), wherein the first and second video cards operate concurrently to output graphics data to a display device (Col. 1 lines 40-57; Col. 4, lines 15-19). This would be obvious for the same reasons given in the rejection for Claim 41.

27. Claims 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) and Peleg (US006557065B1) in view of Grimaud (US005546530A).

28. With regard to Claim 50, Levy and Peleg are relied upon for the teachings as discussed above relative to Claim 1.

However, Levy and Peleg do not teach that a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section. However, Grimaud describes a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section (Col. 2, lines 40-44, 53-65).

It would have been obvious to modify the devices of Levy and Peleg so that a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section as suggested by Grimaud because Grimaud suggests that this ensures that a single graphics element is not overburdened with its rendering task by allowing dynamic adjustment of each graphics element so that the graphics elements take approximately the same time to render their respective images, and the video cards can operate on these divided sections in parallel, therefore allowing different graphics machines to be connected together to render complex images faster than any one of them taken separately would be able to render (Col. 5, line 55-Col. 6, line 12; Col. 7, lines 10-40).

29. With regard to Claim 51, Claim 51 is similar in scope to Claim 50, and therefore is rejected under the same rationale.

30. With regard to Claim 52, Claim 52 is similar in scope to Claim 50, and therefore is rejected under the same rationale.

Prior Art of Record

Gary Brown, "How Motherboards Work", http://electronics.howstuffworks.com/motherboard.htm/printable.

"CPU", http://www.webopedia.com/TERM/C/CPU.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner